UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,450	08/26/2003	Michael Doogue	ALLEG-039PUS	5775

22494 7590 04/01/2008

DALY, CROWLEY, MOFFORD & DURKEE, LLP
SUITE 301A
354A TURNPIKE STREET
CANTON, MA 02021-2714

EXAMINER
NGO, HUNG V

ART UNIT	PAPER NUMBER
2831	

NOTIFICATION DATE	DELIVERY MODE
04/01/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@dc-m.com
amk@dc-m.com

Office Action Summary	Application No.	Applicant(s)	
	10/649,450	DOOGUE ET AL.	
	Examiner	Art Unit	
	Hung V. Ngo	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-18,29-33 and 36-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-11,13-18,29,30,32,33 and 36-41* is/are rejected.

7)☒ Claim(s) *12 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01-27-08 & 02-13-08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The reference No. 2007/026749 does not match any documents.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4-7, 13, 14, 17, 18, 29, 30, 32, 33, 39-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishida (EP 0867725).

Ishida disclose a lead frame having a plurality of leads (1) and having a current conductor portion (1a) comprising a coupling of at least two of the leads, each one of the leads having a respective length;

a substrate (6) having first and second opposing surfaces, the first surface proximate to the current conductor portion and the second surface distal from the current conductor portion, wherein at least some of the leads of said lead flame are electrically coupled to said substrate; and

one or more magnetic field transducers (3) disposed on the first surface of said substrate, wherein said substrate and said lead frame are relatively disposed in a flip-chip arrangement resulting in the current conductor portion being proximate to said one or more magnetic field transducers, and further resulting in an increased sensitivity of the integrated circuit to a magnetic field (Fig 5)

Re claim 4, wherein the curent conductor portion further comprises a conductive clip (2) coupled to the at least two of the plurality of leads.

Re claim 5, wherein said substrate is disposed having the first surface of said substrate above said conductive clip and the second surface of said substrate above the first surface (Fig 5).

Re claim 6, wherein said substrate is disposed having the first surface of said substrate below said conductive clip and the second surface below the first surface (Fig 5).

Re claim 7, wherein a thickness of the conductive clip is selected in accordance with a current passing through the conductive clip (Fig 5).

Re claim 14, further comprising at least one amplifier disposed on said substrate (page 5, line 40).

Re claim 17, further comprising a flux concentrator disposed proximate said one or more magnetic field transducers (page 5, lines 4-6).

Re claim 18, further comprising a flux concentrating layer disposed proximate the second surface of said substrate (page 5, lines 4-6).

Re claim 39, wherein at least some of the leads of said lead frame are electrically coupled to said substrate (Fig 5)

Re claim 40, wherein each one of the leads has a bend in a direction selected to result in each one of the leads being closer to the first surface of said substrate than to the second surface of said substrate throughout a length of the lead (Fig 5).

Re claim 29, Ishida disclose an integrated circuit, comprising:

a lead frame having a plurality of leads (1) and having a current conductor portion (1a) comprising a coupling of at least two of the plurality of leads (Fig 5), wherein the coupling of at least two of the plurality of leads comprises
a loop, the at least two of the leads and the loop forming a continuous electrical path entirely formed of lead frame (Fig 5)

a substrate (6) having first and second opposing surfaces, the first surface proximate to the current conductor portion and the second surface distal from the current conductor portion, wherein at least some of the leads of said lead flame are electrically coupled to said substrate (Fig 5); and

one or more magnetic field transducers (3) disposed on the first surface of said substrate and proximate to the loop such that the one or more magnetic field transducers are responsive to a current flowing through the loop (Fig 5).

Re claim 30, wherein at least one of the one or more magnetic field transducers is disposed within an inner dimension of the loop (Fig 5).

Re claims 13, 32, wherein at least a part (1a) of the current conductor portion has a thinned rectangular cross section having a smallest dimension less than a thickness of other portions of said lead frame, the thinned rectangular cross section taken through a thickness direction of the current conductor portion, the thinned rectangular cross section resulting in an increased magnetic field (page 5, lines 4-6) proximate to the current conductor portion and therefore, proximate to said one or more magnetic field transducer (Fig 5)

Re claim 33, wherein each one of the leads has a bend in a direction selected to result in each one of the leads being closer to the first surface of said substrate than to the second surface of said substrate throughout a length of the lead (Fig 5).

Re claim 41, wherein said substrate and said lead frame are relatively disposed in a flip-chip arrangement resulting in the current conductor portion being proximate to said one of more magnetic field transducers, and further resulting in an increased sensitivity of the integrated circuit to a magnetic field.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida in view of Yanagawa et al (US 2001/0028115).

The teaching as discussed above does not disclose at least one bonding pad (35) coupled to a corresponding one of the plurality of leads (36) with a bond wire (34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made modify the connection of Ishida by employing bonding pad and bond wire for releasing stress to the chip as taught by Yanagawa et al (abstract).

Claims 9, 36, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida in view of Williams (US 2005/0230843).

The teaching as discussed above does not disclose wherein said substrate is coupled to said lead frame with a selected one of a solder ball, a gold bump, a eutectic and high lead solder bump, a no-lead solder bump, a gold stud bump, a polymeric conductive bump, or an anisotropic conductive paste coupled to a corresponding one of the plurality of leads.

William teaches the use of the substrate is coupled to said lead frame with a selected one of a solder ball, a gold bump, a eutectic and high lead solder bump, a no-lead solder bump, a gold stud bump, a polymeric conductive bump, or an anisotropic conductive paste (12) coupled to a corresponding one of the plurality of leads (20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made modify the connection of Ishida by employing conductive bump for the purpose having a low profile chip package.

Claims 10, 11, 15, 16, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida in view of Meyer et al (US 2002/0179987).

The teaching as discussed above does not disclose wherein at least two of said one or more magnetic field transducers are disposed on opposite sides of the current conductor portion axis (re claim 10), wherein at least two of said one or more magnetic field transducers are rotated relative to each other for providing predetermined voltage output polarities (re claim 11), at least two of said one or more magnetic field transducers (re claim 15), four of said one or more magnetic field transducers (re claim 16).

Meyer et al teaches the use of two or more magnetic field transducers (20, 22) positioned in chip (48, 50) for detecting an angle of rotation [0009]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include two or more magnetic field with the structure of Ishida for the purpose of detecting an angle of rotation.

Allowable Subject Matter

Claims 12, 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 1, 29 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung V. Ngo whose telephone number is (571) 272-1979. The examiner can normally be reached on Monday to Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on (571) 272-2800 EXT 31. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hung V Ngo/
Primary Examiner, Art Unit 2831